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THRESHOLD VOLTAGE MODEL OF SiC SHORT CHANNEL MOSFET's WITH DEEP IMPURITY LEVELS AND TRAPS

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1. Introduction

Recently, MOSFET's (MESFET's), IMPATT diodes, fast resonant tunneling diodes and tunnel emitter transistors as well as many other devices made of silicon carbide and having excellent DC and RF performance have been demonstrated [1-5]. They are in the stage of lab investigation and need further improvement. On the other hand, during different technological processes deep levels and trap centers with the large varying concentrations and energy distributions are formed in crystals. In particular, the donor center energy is changed from $(E_c-0.13)$eV to $(E_c-1.0)$eV, acceptor energy distribution from $(E_v+0.5)$eV to $(E_v+1.19)$eV and the capture cross-section of traps is changed in the range 10^{-13}-10^{-17} cm^2 in SiC. It is known that controlled doping with impurities creating deep levels and traps leads to the redistribution of internal electric fields and permits to improve static and dynamic characteristics of devices. In previously investigations of MOSFET's (MESFET's on Si, GaAs), it is assumed that impurities create only shallow levels and that at room temperature all impurities are in quite ionized condition. And there are no investigations on the influence of traps on the threshold voltage and other characteristics of SiC-MOSFET's. We are underline that both these statements are not valid assumptions for SiC devices.

We pointed out that the existence of a high concentration defect (traps) and non-ionized deep impurity levels leads to the increase in the depletion layers of source and drain regions of MOSFET's and we can't neglect the source and drain depletion regions for short channel. These states are capable of trapping considerable density of electrons, reduce the current and charge mobility in the channel. Moreover, in short and narrow channel case the degree of influence of deep impurity and trapping levels on the channel modulation effects will be significantly increased.

It is, however, urgent to investigate the influence of different defects (traps) and deep impurity donor (acceptor) levels existing in the material itself or being induced during devices

processing on the device performance, particularly on the threshold behavior for the short channel SiC-MOSFET's. The short channel effects which arise as a consequence of two-dimensional potential distribution, high electric field and carrier quantization (2DEG effects) in the channel region require an accurate and new efficient design methods of modeling all fundamental parameters of MOSFET's.

In this report we present a new model of short channel SiC MOSFET's threshold voltage modeling, based on detailed analysis of the charge conservation law in the region bounded by the gate electrode and the semiconductor bulk.

2. Theory

By presenting the channel as a two- dimensional triangular- form quantum well (Fig.1) and solving two- dimensional Poission's equation

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=-\frac{q}{\varepsilon_1}\left\{p(y)-n_{ts}-n_{tt}-N_a^-n_{ij}(y)\right\}$$

and one-dimensional Schrodinger's equation

$$-\frac{\hbar^2}{2}\frac{d}{dy}\left(\frac{1}{m_j^*(y)}\cdot\frac{d}{dy}\right)\chi_{ij}(y)+U(y)\chi_{ij}(y)=E_n\chi_{ij}(y),$$

where $\psi(x,y)$ is the surface potential, q is the electron charge, ε_1 is the dielectric permittivity of SiC, $p(y)$ is the hole concentration in the substrate, n_{ts} is the surface states trapped electron concentration, n_{tt} is the channel region trapped electron concentration, N_a^- is the concentration of ionized acceptors, $n_{ij}(y)$ is the electron density for the energy level E_n, $\hbar$ is the reduced Planck constant, $m_j^*(y)$ is the effective mass, $U(y)$ is the potential energy $(U(y)=-q\psi(x,y)+\Delta E_C(y),\ \Delta E_c(y)$, is the band offset at the interface), $\chi_{ij}(y)$ is the envelope wave function, subscript i denotes the energy sub-band and subscript j denotes the semiconductor valley.

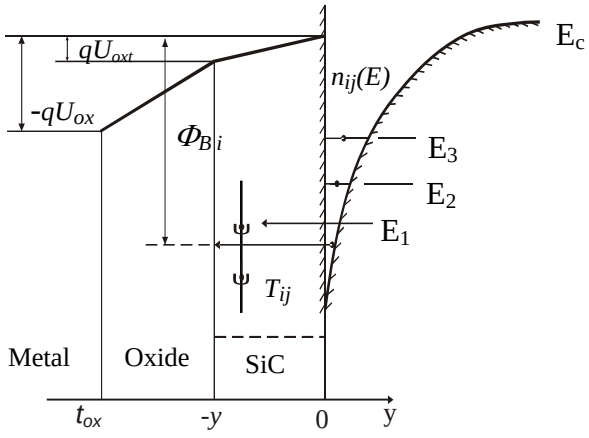


Fig. 1. Band diagram of the SiC- SiO2 system in the presence of a trap.

For the threshold voltage we obtain

the following expression:

$$U_g = \Phi'_{ms} - \frac{Q_{ox}(y)}{C_{ox}} + \frac{1}{L}\int_0^L \psi(x,y)\,dx + \frac{1}{C_{ox}L}\left\{\int_0^L Q_B(y)\,dx + \int_0^L Q_n\,dx + \int_0^L Q_t\,dx\right\},$$

where $U_{FB} = \Phi'_{ms} - \frac{Q_{ox}(y)}{C_{ox}}$ is the flat-band voltage, Φ'_{ms} is the gate-substrate work function difference, $Q_{ox}(y)$ is the oxide fixed charge, C_{ox} is the per- unit- area oxide capacitance, L is the channel length, $Q_B(x,y)$ is the total semiconductor charge, $Q_t(x,y)$ is the total charge trapped in traps, $Q_n(x,y)$ is the free electron charge in the inversion layer.

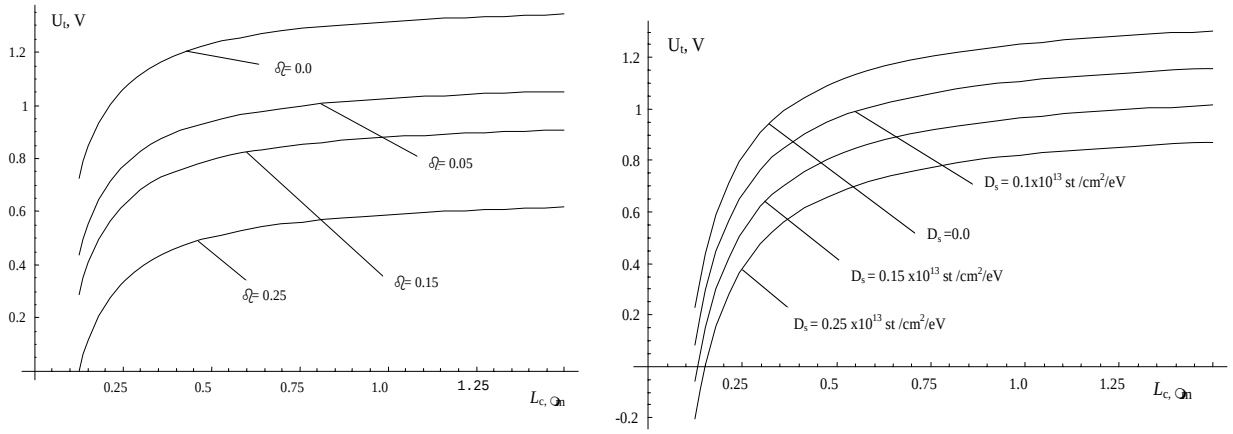
3. Conclusion

The numerical calculations have been carried out by the "MatLab" program with the following parameters: the p-n junction depth $r_j \sim 0.09\,\mu$m [1], the oxide thickness 5-15 nm, the channel length L = 0.25 - 1 μm [1, 5], UFB = –1.7 V (for n-channel SiC-Pt system), the channel thickness 30- 300 Å and the density of surface states Ds~10^{13}-10^{14} states/cm^2/eV [1] , the substrate doping $N_a \sim 10^{15}$ - 10^{17} cm^{-3} [1,3], the trap concentration in the bulk $N_t \sim 10^{12}$ - 10^{14} cm^{-3}, the trap concentration in the oxide $N_{tox} \sim 10^{12}$ - 10^{13} cm^{-3} [5,7,8], the deep acceptor activation energy $\Delta E_a \approx 0.1$- 0.26 eV [7,8], electron affinity $\chi \approx$ 4.1 eV, the effective mass $m^*_{djc} = 0.45 m_0$ (4H-SiC) [2], the built in potential U_{Bi}~1.7- 2.3 V, depletion layer width in the channel region $h_c \sim 0.15\,\mu$m, the bulk Fermi potential [3]

$$\Phi_B = kT \ln\left\{\frac{1}{2}\left[\frac{N_a^-}{n_i} + \left[\left(\frac{N_a^-}{n_i}\right)^2 + 4\right]^{1/2}\right]\right\},$$

where *k* is the Boltzmann constant, *T* is the absolute temperature, ni is the intrinsic concentration.

The results are shown in Fig. 2. As it is evident from Fig. 2, with increasing trap concentration at the surface and in the channel region, the threshold voltage decreases and the point where the threshold takes place is displaced to the higher value of channel length. We think that this behavior of the threshold is connected with the additional band offset due to trapped charge in surface states and in interface, which leads to a more rapid fulfillment of the threshold condition.



a) b)

Fig.2. Threshold voltage versus channel length for different values of traps concentration (a) and surface states concentration (b).

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